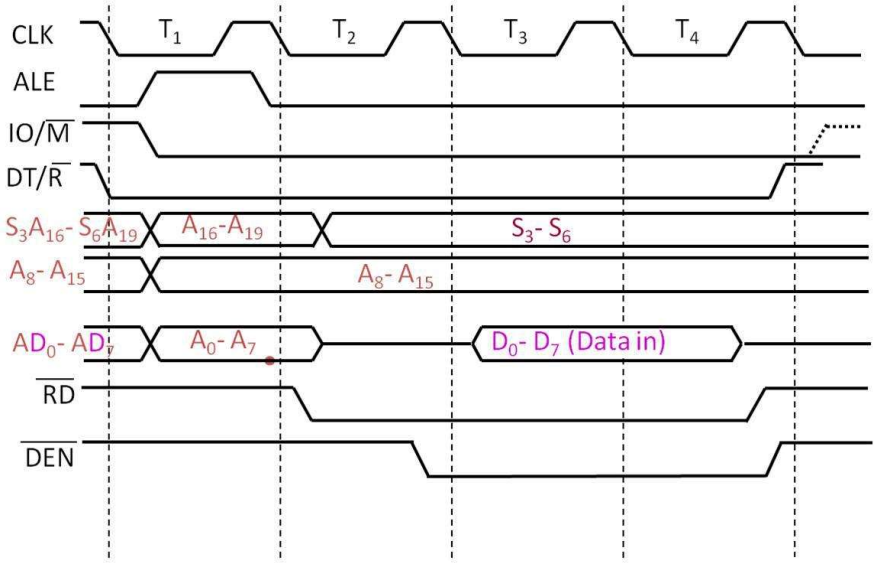
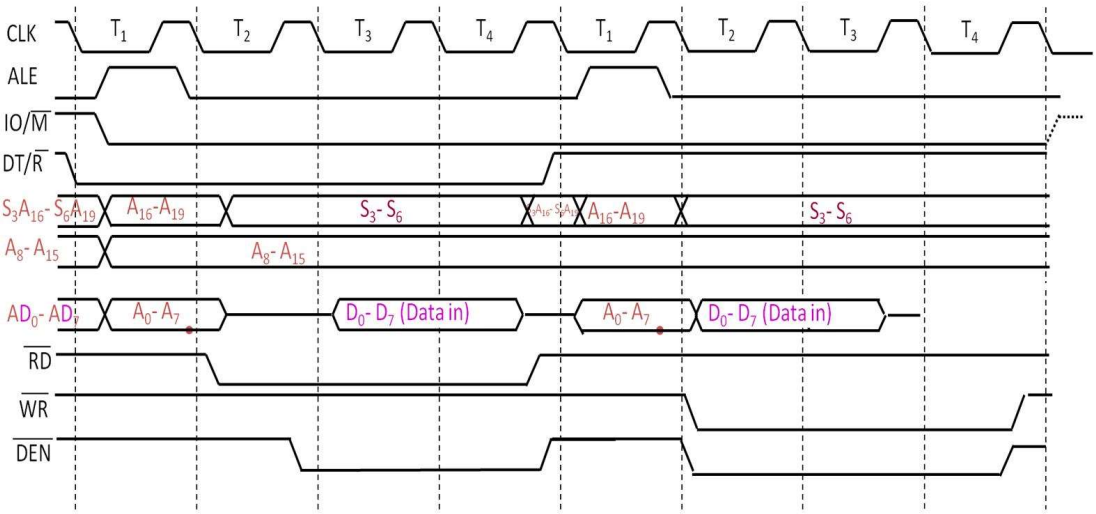
1-1 Assume that; DI=1645h , SI= 4759h , DS= 8000h , data in DS:DI = 1066h , data in DS:SI = 5522h

Draw a system bus timing diagram required to execute the following instructions by the microprocessor 8088;

1- MOV BL, [DI]



2- INC byte ptr [SI]



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2-1- What is the highest address in the 8088's memory address space? The lowest address?

the highest address : FFFFF , THE LOWEST ADDRESS : 00000H

2-2-In relation to interfacing a processor to a memory system with more than one bank.

a. Why a separate write control signal is needed for each bank?

ONCE THE MICROPROCESSOR WRITE A DATA WORD TO THE MEMORY , IT NEEDS TO ACTIVATE THE CORRECT OR THE TARGET BANK, BASED ON THE ADDRESS EVEN OR ODD.

b . Why only one read control signal is needed for all banks?

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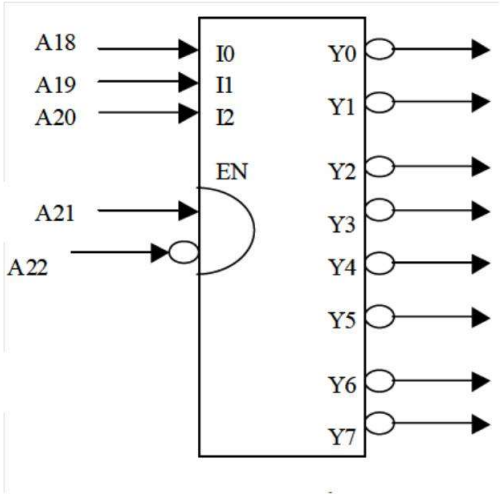
2-3 For the address decoder below:

a. Give the address range of addresses that output Y5 is valid for ?

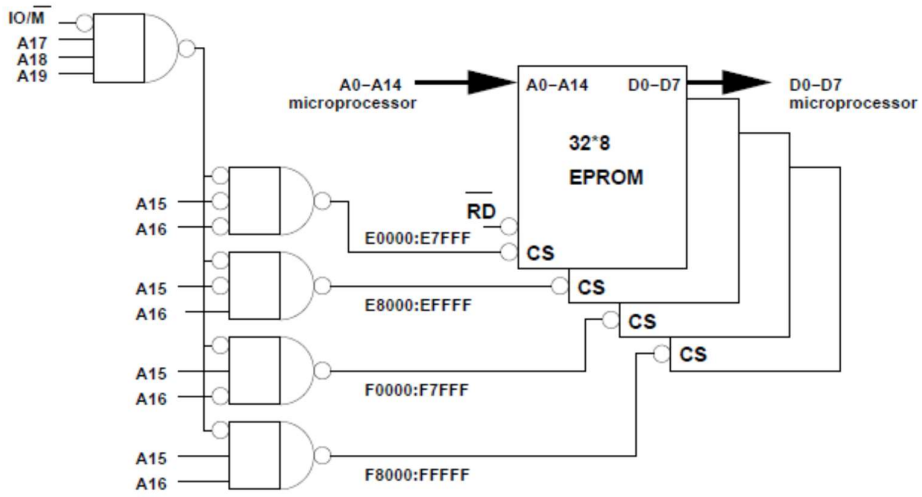
A22	A21	A20	A19	A18	A17	A16	A15- A0	
0	1	1	0	1	0	0	0000	TO
0	1	1	0	1	1	1	FFFF	

b. How many total byte is this address decoder valid for ? (give the answer in Kbyte)

$2^{18} = 2^8 \times 2^{10} = 256$kBYTE



2-4 For an 8088 microprocessor, use the NAND-gate technique (only NAND gate and inverters allowed) to map the upper most eighth (1/8) of the memory (ending at FFFFF) into four identical EPROM chips. Find out the size of suitable EPROM chips. Draw the circuit and indicate the start and the end addresses accessible through each EPROM. Use the RD' and IO/M' control signals of the microprocessor to access memory?



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3-1 Write an ASP to print alphabet characters from A to Z on the screen as follow:

AZ BY CX DW EV FU MT ..... WC XB ZA , using INT21 DOS interrupt

3-2 describe the action taken by 8086 when NMI pin is activated ?

3-2 If the interrupt service routine(ISR) of the interrupt source (INT 10H) has located at a logical address (1500:E308H). Write the instruction required to initialize the interrupt vector table in order to handle this interrupt.

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GOOD LUCK FOR ALL

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